UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/814,928	02/27/1997	VISHRAM P. DALVI	42390.P4024	5243

7590 02/08/2002

LESTER J VINCENT
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025

EXAMINER	
ROBERTSON, DAVID L	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 02/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES
PATENT AND
TRADEMARK OFFICE

Under Secretary of Commerce for Intellectual Property and
Director of the United States Patent and Trademark Office
Washington, DC 20231
www.uspto.gov

Before the Board of Patent Appeals and Interferences

Examiner's Answer

This is in response to appellants' brief on appeal filed January 24, 2002 (with certificate of mailing of October 17, 2001).

Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

Status of Claims

The statement of the status of claims contained in the brief is correct.

Status of Amendments After Final

The appellants' statement of the status of amendments after final rejection contained in the brief is correct.

Summary of Invention

The summary of invention contained in the brief is correct.

Issues

The appellants' statement of the issues in the brief is substantially correct. However, the first § 103 rejection was made in the alternative while the second was not. The changes, using appellants' language as much as possible, are as follows:

A. 1. Whether under 35 U.S.C. § 103(a) claims 31-37 are unpatentable over applicants' admitted prior art ("AAPA").

2. Whether under 35 U.S.C. § 103(a) claims 31-37 are unpatentable over Terada.

B. Whether under 35 U.S.C. § 103(a) claims 31-37 are unpatentable over Leak in view of Terada.

Grouping of Claims

The appellants' statement that claims 31-37 stand or fall together is acceptable.

Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

Terada *et al.*	5,561,628	10/1996
Leak *et al.*	5,937,424	8/1999

Applicants' admitted prior art (AAPA), as found on page 1, line 7-page 3, line 8 of appellants' specification.

New Prior Art

No new prior art has been applied in this Examiner's Answer.

Grounds of Rejection

The following ground of rejection is applicable to the appealed claims.

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were,

at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 31-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art. Applicant's admitted prior art teaches that it was known in the prior art to suspend flash memory erase cycles because of the length of time required for the erase cycle (see specification, lines 1-2). Further, applicants admit that in such devices status registers typically stored data indicative of the current device status, including whether or not an erase operation had been suspended (see figure 1, memory location 104, "ESS"). Applicants also admit that the stored status was output when the device was polled or in response to a "read status register command" (see specification, page 2, lines 3-7). The memory array in applicant's described prior art is understood. Applicants do not admit that suspension of a programming (write) operation was taught in the prior art. However, while a programming (write) operation did not take as long as an erase operation, it still took a significant amount of time relative to a data read operation (7-8 microseconds as opposed to 85 nanoseconds, see specification, page 1, lines 22-25). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified applicant's admitted prior art to have included the ability to suspend programming (write) operations to improve the overall performance of a flash memory device. Such a modification, would clearly have involved the modification of the status register to have included at least one bit to indicate the suspension status of a programming (write) operation (e.g., a "PSS" (or "WSS") bit similar to the admitted

"ESS" bit). Applicants do not discuss the existence in the prior art of a control circuit including a first state machine for receiving commands to access the memory array or the status register and a second state machines to execute the command received by the first state machine. However, such implementation was typical at the time, i.e., a command decoder (i.e., a first state machine) was required to determine what type of command had been received, whether it was a valid command, whether it could have been be executed, etc. If the command could indeed have been executed, the command was typically sent to circuitry specific to the execution of the command (i.e., a second state machine). Clearly applicant's admitted prior art received a command (i.e., when polled or in response to a "read status register" command, see specification, page 2, lines 4-7) and then executed the command (i.e., "the status signal may be sent...via a designated output pin" or "via the data input/output ('I/O') pins", *ibid*). It was inherent that applicant's admitted prior art included the claimed first and second state machines. Further, the admitted prior art programming (write) operation inherently would have included a "byte write" (or "byte program") instruction (claim 32) since that was the typical manner of writing to flash memories. Obviously the "byte write" operation would have been the programming (write) operation to suspend (claim 33). It would also have been obvious that the "status register read" operation of applicant's admitted prior art would have output the contents of the entire status register as modified above, including the program (write) suspend status (claim 34). A device as described above would inherently have included the ability to input "status register read" requests and output status register data (claim 35). Applicant's admitted prior art included the ability to be polled or to

receive a "read status register" command, this it would have been obvious to have retained such abilities (claims 36 and 37).

Claims 31-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terada *et al.* (U.S. 5,561,628). The Terada *et al.* reference teaches, *inter alia*, flash EEPROMs (see figure 3, flash memories 40a through 40d) with the ability to suspend erase cycles, and a status register that outputs an "erase suspend status" signal (see Table 1, bit 6 and Table 2, register SR.6) when the status register is read (see column 10, lines 47-59 and tables 1 and 2). The memory array *per se* is understood. Terada does not teach the suspension of a programming operation. However, while a programming (write) operation does not take as long as an erase operation, it still takes a significant amount of time relative to data read operation. In a particular 8M-bit IC card it "takes one second or less to read all the addresses on one flash memory, 9.6 seconds to write in all the addresses in one flash memory, and 25.6 seconds to erase from all the addresses of one flash memory", see column 5, lines 5-11). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified the memories taught by Terada to include the ability to suspend programming (write) operations to improve the overall performance of a flash memory device. Such a modification, would clearly involve the modification of the status register to include at least one bit to indicate the suspension status of a programming (write) operation (e.g., a "PSS" (or "WSS") bit similar to the "ESS" bit). Terada does not discuss a control circuit including a first state machine for receiving commands to access the memory array or the status register and a second state

machines to execute the command received by the first state machine. However, such implementation is typical, i.e., a command decoder (i.e., a first state machine) is required to determine what type of command has been received, whether it is a valid command, whether it can be executed, etc. If the command can indeed be executed, the command is typically sent to circuitry specific to the execution of the command (i.e., a second state machine). Clearly Terada's flash memories receive a command (i.e., "can be read", see column 10, lines 53-55) and then executes the command (i.e., "via a data bus for transmitting signals D0 to D15", *ibid*). It is inherent that Terada includes the claimed first and second state machines. Further, each of the Terada flash memories operates in a "byte write" (or "byte program") mode (see table 2, SR.4, claim 32). Obviously the "byte write" operation would be the programming operation to suspend (claim 33). It is also obvious that Terada's status register read operation would output the contents of the status register as modified above, including the write suspend status (claim 34). A device as described above would inherently include the ability to input requests and output data (claim 35). Terada's flash memories clearly can be polled or otherwise read (claims 36 and 37).

Claims 31-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leak *et al.* (U.S. 5,937,424) in view of Terada *et al.* (U.S. 5,561,628). The Leak reference teaches a memory device which includes a memory array (understood), a register to store status information (see figure 7B, status register 142), a control circuit including a command decoder (first state machine) and a second state machine (see figure 7B, any of elements 190, 192, 194, 195, 196 and 198. There is little description about the status register 142. However, with respect to the

ostensibly similar prior art status register (element 42, figure 1), the Leak reference states: "The status register 42 is also coupled to provide data to the output multiplexer 60 for providing status data to the data I/O pins 12 of the flash EPROM responsive to a read status operation." (See column 2, lines 46-49.) The reference further teaches that it is advantageous to be able to suspend both erase and write (program) operations in order to improve system performance. More specifically, the Leak reference validates the reasoned findings stated by the examiner in the rejections above:

> For example, if a processor were performing a program operation to write a byte of data to the flash EPROM, and subsequently the processor requested that the flash EPROM perform a read operation in order to perform a code fetch, i.e., a read of code to get new instructions for the processor to execute, the read operation may be delayed up to 100 microseconds waiting for the program operation to complete. This causes the processor to stall--the processor remains idle until it receives new instructions. Such a delay to read code would be unacceptable in a system that requires code fetches to be performed in less time than the maximum program operation time. (Column 3, lines 56-67.)

The Terada reference has been discussed in the rejection above. It teaches a status register that includes an "ESS" bit to indicate the erase suspend status of the device. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modeled the Leak status register after the Terada status register to include an "ESS" bit to indicate that an erase operation has been suspended, and to have further modified the status register to include a "WSS" bit (or "PSS" bit) to indicate that a write (program) operation has been suspended. By comparison to the prior art, it appears that the

Leak device operates in byte write mode and that the byte write operation is suspended (claims 32 and 33). In keeping with the modification above, note that Terada teaches that if ESS = 1, an erase operation is suspended, if ESS = 0, then no erase is suspended. The modification suggested by the examiner above would, by analogy, indicate that if WSS = 1, then a write operation is suspended and if WSS = 0, then no write operation is suspended (claim 32). The Leak command decoder has an input and clearly receives a status read signal to activate read status circuitry 198 (see figures 7A and 7B). The status register outputs the status data on line RY/BY# (see figure 7B), upon receiving a "status read operation" (claims 36 and 37).

New Ground of Rejection

This Examiner's Answer does not contain any new ground of rejection.

Response to Argument

a. Applicants' Admitted Prior Art...

Contrary to appellants' assertion, AAPA does not teach away from the suspension of a program operation. Rather, AAPA teaches that the time required for a write operation (7-8 microseconds) is two orders of magnitude larger than that of a read operation (85 nanoseconds). Clearly, interrupting a write operation to perform a read operation would have little impact on the write operation, whereas delaying the read operation for the duration of an entire write operation

would clearly adversely impact the read operation. Appellants' statement regarding the examiner's reliance on Terada being flawed in two respects is also not agreed with. While the differences between the writing time (9.6 seconds) and erasing time (25.6 seconds) in are not as dramatic as stated by AAPA, the fact that Terada is directed to testing the memory chip obscures the real significance. Because Terada is discussing flash memory, an entire block of memory is erased in a single operation that takes 25.6 seconds. However, Terada discusses a conventional test method which programs the memory with individual byte-writes to each and every location in the memory, one at a time. The time required to write to each memory location, one byte at a time (hundreds, maybe thousands of write operations) is 9.6 seconds. Thus, the Terada reference does not depart significantly from the teachings of AAPA. What appellant misses, however, is that the motivation flows from the difference between the time required for a write operation and a read operation, which Terada teaches to be at least an order of magnitude different. In any event, the record with respect to AAPA and Terada clearly shows that it was known that it took significantly longer to erase a memory block than it took to program a single memory location and that it took significantly longer to program a memory location than it took to read a memory location. Also the record shows that it was well known to suspend an erase operation to reduce the overall pendency of a read operation, and further it was known to include an indicator in a status register that indicated whether an erase operation had been suspended, or not.

b. Terada is not Analogous...

Terada was relied upon for the discussion of the time differences between erasing a block of flash memory, writing to each and every location in said memory, and reading each and every location in said memory, and the existence in the prior art of an "erase suspend status" bit in the status register. While it is true that Terada then goes on to solve a problem related to testing each and every memory location on the chip, appellants' argument is nevertheless specious. Both references would be of interest to any person dealing with the design of flash memory, and the art is thus in the same field of endeavor. Further, at the risk of being repetitious, Terada was being relied upon, not for any inventive material disclosed but rather, for establishing the state of the art with respect to read and write times of flash memory and an "ESS" bit in the status register.

c. Neither Applicants' Admitted Prior Art Nor Terada Teach...

Appellants' statement that for claims "to be rendered obvious, the AAPA or Terada must disclose or suggest each and every limitation of the claim" is not completely correct. All of the limitations in the claims must be addressed in the rejection, but the conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference, *In re Bozek*, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969). See also *In re Fox*, 471 F.2d 1405, 176 USPQ 340 (CCPA 1973)(§ 103 rejection in which no art was cited). The claims were rejected under § 103 over AAPA or Terada, not § 102. Starting from where each of the references leave off, it is the judgement of this tribunal that in view of the facts of record, as reiterated above, the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. The rejection presents reasoned findings as to why one of ordinary skill, upon learning of the suspension of an erase operation and the reasons therefor, would have been motivated to have suspended a write operation for the same reason (i.e., they both take much longer than a read operation by itself; forcing a read request to wait for either operation to finish seriously degrades overall system performance). Note that the level of ordinary skill in the art of designing memory chips and circuits was extremely high, and included advanced college degrees and several years of on the job training; it is reasonable to expect that such individuals were able to synthesize ideas and extrapolate from general concepts. As to the alleged deficiency of a control circuit to update the register and control the output of a status signal, both AAPA and Terada provide for updating the status register and outputting the status register. The modification of status register to include a "write suspend status" bit does not require any significant change to the control circuits that are inherent to AAPA and Terada.

d. Terada in Combination with Leak Fails...

Again appellants misstate the law. Further, while Leak does not overtly disclose a control circuit to update the status register, the fact that it has a status register implies that there is circuitry to update it. The reference does teach a control circuit to output the status register (see element 198, compare element 98). Further, the fact that the reference suggests that the device outputs the contents of the register in response to a "read status operation" further implies that if

it is in a "write suspend status", that such would have been indicated by the "read status operation."

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

David L. Robertson

Conferees:

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187

RIE

REBA I. ELMORE
PRIMARY EXAMINER
GROUP 2800